

Application No.: 09/990,397

Docket No.: JCLA7289

In The Claims:

Claim 1. (currently amended) A flash memory structure, comprising:

a tunneling oxide layer located upon a substrate;

a floating gate located upon the tunneling oxide layer;

a first oxide layer located upon the floating gate;

a high dielectric constant dielectric layer located upon the first oxide layer, wherein a dielectric constant of the high dielectric constant dielectric layer is greater than 8 and a band gap value of the high dielectric constant dielectric layer is less than a band gap value of silicon oxide;

a second oxide layer, located upon the high dielectric constant dielectric layer, wherein, together with the first oxide layer and the high dielectric constant dielectric layer, a dielectric stacked layer is formed;

a control gate formed on the second oxide layer of the dielectric stacked layer; and

a source/drain region located in the substrate on the two sides of the floating gate.

Claims 2-3 (canceled)

Claim 4. (original) The flash memory structure as defined in claim 1, wherein the high dielectric constant dielectric layer is a single layer including one material selected from the group consisting of Al_2O_3 , Y_2O_3 , ZrSi_xO_y , HfSi_xO_y , La_2O_3 , ZrO_2 , HfO_2 , Ta_2O_5 , Pr_2O_3 and TiO_2 .

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Claim 5. (original) The flash memory structure as defined in claim 1, wherein the high dielectric constant dielectric layer is a layer including a mixed material any one selected from the group consisting of Al_2O_3 , Y_2O_3 , ZrSi_xO_y , HfSi_xO_y , La_2O_3 , ZrO_2 , HfO_2 , Ta_2O_5 , Pr_2O_3 and TiO_2 .

Claim 6. (original) The flash memory structure as defined in claim 1, wherein the material of the high dielectric constant dielectric layer is stacked layer, each layer of the stacked layer including one selected from the group consisting of Al_2O_3 , Y_2O_3 , ZrSi_xO_y , HfSi_xO_y , La_2O_3 , ZrO_2 , HfO_2 , Ta_2O_5 , Pr_2O_3 and TiO_2 .

Claim 7. (currently amended) A flash memory structure, comprising:

a tunneling oxide layer located upon a substrate;

a floating gate located upon the tunneling oxide layer;

a first oxide layer located upon the floating gate;

a high dielectric constant dielectric layer having a dielectric constant greater than 8 located upon the first oxide layer, wherein, together with the oxide layer, a dielectric stacked layer is formed, and a band gap value of the high dielectric constant dielectric layer is wide or wider than a band gap of silicon oxide;

a control gate formed on the high dielectric constant dielectric layer of the dielectric stacked layer; and

a source/drain region located within the substrate on the two sides of the floating gate.

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Claims 8-9 (canceled)

Claim 10. (original) The flash memory structure as defined in claim 7, wherein the high dielectric constant dielectric layer is a single layer including one material selected from the group consisting of Al_2O_3 , Y_2O_3 , ZrSi_xO_y , HfSi_xO_y , La_2O_3 , ZrO_2 , HfO_2 , Ta_2O_5 , Pr_2O_3 and TiO_2 .

Claim 11. (original) The flash memory structure as defined in claim 7, wherein the high dielectric constant dielectric layer includes a mixed material selected from any one of the group consisting of Al_2O_3 , Y_2O_3 , ZrSi_xO_y , HfSi_xO_y , La_2O_3 , ZrO_2 , HfO_2 , Ta_2O_5 , Pr_2O_3 and TiO_2 .

Claim 12. (original) The flash memory structure as defined in claim 7, wherein the high dielectric constant dielectric layer is a stacked layer, each layer of the stacked layer including one selected from the group consisting of Al_2O_3 , Y_2O_3 , ZrSi_xO_y , HfSi_xO_y , La_2O_3 , ZrO_2 , HfO_2 , Ta_2O_5 , Pr_2O_3 and TiO_2 .

Claim 13 (canceled)